

VIDEO SIGNAL TIMING IN A MULTI-FORMAT ENVIRONMENT

Background of the Invention

This invention relates to video signal timing in a
5 multi-format environment.

Until quite recently, the rules of the United States
Federal Communications Commission (FCC) required that video
material should be broadcast using the NTSC signal format.
The NTSC video format is an interlaced format, in which each
10 frame is composed of two fields. The frame rate of the NTSC
video format is $30/M$ frames/sec where M is a data rate
divisor and is equal to 1.001.

In a television broadcast facility, several video signal
sources, each generating a signal in NTSC format, are
15 connected to respective inputs of a router, which supplies
the video signals to selected video signal destinations. The
various signal sources are controlled by a common timing
signal so that they are in phase.

The router is composed of multiple input buses,
20 connected to the sources respectively, multiple output buses,
connected to the destinations respectively, and an array of
crosspoint switches that are operable selectively for
connecting any one input bus to any selected set of one or
more output buses. The state of the ij th crosspoint switch
25 is ON (it connects output bus j to input bus i) or OFF (it
isolates output bus j from input bus i). The router includes
a memory having an addressable location associated with each
crosspoint switch. During each active interval of the video
signal, the memory is addressed to store in each location the
30 desired state of the corresponding crosspoint during the next
active interval. The desired state may be the same as the
current state or it may be the opposite state. During the
vertical blanking interval, the contents of the memory are
used to update the entire array of crosspoint switches.

35 In order to minimize degradation of the output signals
of the router, the update is made consistently on the same
line of the video signal frame. This line is referred to as
the switch line, and the time at which the crosspoints are

FOI b6 b7C b7D

updated is referred to as the switch point. Nominally, the switch point is halfway through the switch line, but SMPTE RP-168 defines a window of $\pm 5 \mu s$.

Since the NTSC video format is an interlaced format,
5 there are two vertical blanking intervals, and hence two switch lines, per frame. In each field, the switch line is the first line of the vertical blanking interval after the equalizing pulses. The switch line is identified by continuously monitoring the video signal to find vertical
10 sync, and counting lines until the first line after the equalizing pulses.

Current rules of the FCC allow broadcast of video material in a high definition (HD) format, but require that a television broadcaster who broadcasts video material in an HD
15 format should broadcast the same material in standard definition (SD) NTSC format. One way for a broadcaster to meet this requirement would be to generate the video material for broadcast in the HD domain and, concurrently with broadcast of the HD material, convert the HD material to SD
20 and broadcast the SD material. An alternative, which may be attractive for some purposes, would be to receive the source material in both formats, process the SD material in an SD path to generate the SD broadcast stream and concurrently process the HD material in a separate, parallel HD path to
25 generate the HD broadcast stream, and broadcast the SD material and the HD material simultaneously.

Although the SD video signals that are currently broadcast are analog formats, the HD signals are in digital format and almost all of the processing of SD and HD video
30 signals is conducted in the digital domain.

At least thirteen digital HD signal formats, designated by SMPTE 292M Format ID's A-M, have been defined for HD video signals. Several of the format parameters for these digital high definition video signals are listed in Table I.

TABLE I

Reference SMPTE Standard	260M		295M	274M								296M	
Format ID	A	B	C	D	E	F	G	H	I	J	K	L	M
Lines per frame	1125	1125	1250	1125	1125	1125	1125	1125	1125	1125	1125	750	750
Total active lines	1035	1035	1080	1080	1080	1080	1080	1080	1080	1080	1080	720	720
Frame rate (Hz)	30	30/M	25	30	30/M	25	30	30/M	25	24	24/M	60	60/M
Fields per frame	2	2	2	2	2	2	1	1	1	1	1	1	1

The U.S. broadcast facilities that simultaneously broadcast HD and SD streams have each selected either format E or format M for digital HD material. Format E is a 30/M frame/sec, 1125 lines/frame interlaced format and format M is a 60/M frame/sec, 750 lines/frame progressive scan format.

- 15 For some of the digital HD signal formats, there are equivalent analog signal formats in which the blanking interval includes equalizing pulses. Depending on the format, the equalizing pulses occur in the first five or six lines of the vertical blanking interval. With respect to a
- 20 digital signal format having a corresponding analog format, it has been proposed that the switch line should be the first line after the vertical blanking interval. It has also been proposed that the switch line for a digital signal format for which there is no corresponding analog format should be the
- 25 same line as the switch line for the closest digital format for which there is a corresponding analog format.

- In video post production, a router is used to assemble source material to produce a video stream which is supplied to a broadcast facility to include in a broadcast stream.
- 30 For example, in post production several brief scenes might be assembled to form a commercial message, which the broadcaster combines with other commercial messages and program material to generate the broadcast stream. In post production, the segments of the program source material may be in different
- 35 formats. It may be necessary to combine a segment of a first format with a segment of a second format and produce a program in a third format. Much of the material used in post production is based on film, which is 24 frames/sec.

FOUO 20250124 1600

5

15

20

Summary of the Invention

30

It has been suggested in accordance with the invention that it would be desirable to switch HD video data in the SMPTE 292 domain instead of using SMPTE 292 only as an interface standard and converting the SMPTE 292 signal to
 5 Format E or M, for example, for switching. However, a barrier to implementation of this suggestion is that it is not possible to distinguish source format in the SMPTE 292 domain and therefore it is not possible to determine the proper switch point.

10 For the time being, it will be assumed for the sake of simplicity that the value of M is one, not 1.001. Under this assumption, the frame rate of the NTSC signal is 30 Hz and the frame rates of formats E, K and M are 30 Hz, 24 Hz and 60 Hz respectively.

15 It has been observed in accordance with the invention that there is a predictable and repeating sequence of time offsets between a signal having a frequency of 30 Hz (or an integer multiple of 30 Hz) and a signal at a frequency of 24, 25 or 60 Hz. Accordingly, with a master clock signal running
 20 at 30 Hz, or an integer multiple of 60 Hz, it is possible to set switch points not only for 30 frame per second material but also for 24, 25 and 60 frame material provided that the different signal sources have a known time offset, which may be zero, at an arbitrary time t_{ref} . In this event, the switch
 25 lines of each format occur at exactly predictable points in time in a repeating sequence that is reset every second.

In accordance with the present invention there is provided a method of operating a video router in a plant including at least first and second video sources which
 30 provide first and second digital video signals respectively at integer related frame rates, said method including operating the first and second video sources so that the first and second video signals are aligned at a reference time, and defining switch points for updating the router by
 35 measuring lapse of time from said reference time.

FOUO "SECRET"

Brief Description of the Drawings

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, to the accompanying drawings, in
5 which

FIG. 1 is a simplified block diagram of a first television broadcast facility in accordance with the present invention,

FIG. 2 is a simplified block diagram of a second
10 television broadcast facility in accordance with the present invention, and

FIG. 3 is a simplified block diagram of a television post production facility in accordance with the present invention.

15

Detailed Description

FIG. 1 illustrates a broadcast facility including three video sources 10, designated more specifically Source A, Source B and Source C. Source A generates an SD NTSC signal
20 whereas Sources B and C generate HD signals in the broadcaster's selected HD digital format, such as SMPTE Format E. The output signals of the sources are supplied to a format converter 14, which generates an HD signal from the SD input signal and generates SD signals from the HD input
25 signals, and converts the SD signals to SMPTE 259 format and the HD signals to SMPTE 292 format. The SD signals are supplied to an SD router 18 and the HD signals are supplied to an HD router 22. The sources operate under control of a master clock generator 24, which generates a master clock at
30 60 Hz, such that at a selected time t_0 , the start of line 1, field 1, frame 1 of the three signals, generated by the three sources respectively, are aligned. The master clock MCLK is supplied to the format converter 14 and is used to generate local clock signals for controlling the operations performed
35 by the format converter. By using the master clock MCLK to control all operations performed by the format converter, and using delays if necessary to compensate for processing and propagation time, the output signals of the format converter

T06280-22460

are aligned at time t_1 , where $t_1 + t_0$ represents delay from the outputs of the sources 10 to the outputs of the format converter 14.

The SD router provides SD output signals SDX and SDY by switching among its input signals SDA, SDB and SDC. Similarly, the HD router 22 provides output signals HDX and HDY by switching among its input signals HDA, HDB and HDC. The video contents of the signals HDX and HDY correspond to the contents of the signals SDX and SDY respectively.

The master clock signal MCLK is also supplied to an SD offsets circuit 26, which employs delay elements and multiplexers to generate two SD router switching clock signals SDCLK1 and SDCLK2, and to an HD offsets circuit 30, which employs delay elements and multiplexers to generate two HD router switching clock signals HDCLK1 and HDCLK2. The router switching clock signals are used to control updating of the crosspoints of the two routers respectively.

The two signals SDCLK1 and SDCLK2 each have a frequency of 30 Hz but they are offset in time. The signal SDCLK1 is used to update the crosspoints of the router 18 during the blanking interval of field 1 and has an active clock edge occurring halfway through line 1 of each frame, at about $t_1 + nH + 31.75\mu s$, where n represents frame number, and the signal SDCLK2 is used to update the crosspoints during the blanking interval of field 2 and has an active clock edge occurring halfway through line 263 of each frame, at about $t_1 + nH + 16,730.16\mu s$. The switch point of field 1 therefore occurs halfway through line 1 and the switch point of field 2 occurs halfway through the first complete line of field 2. It will be appreciated that the interval between the switch points for field 1 and field 2 is not equal to half the frame interval and therefore the 60 Hz clock cannot be used alone to time both switch points.

Similarly, the two signals HDCLK1 and HDCLK2 each have a frequency of 30 Hz but they are offset in time. The signal HDCLK1 is used to update the crosspoints of the router 22 during the blanking interval of field 1 and has an active clock edge occurring halfway through line 1 of each frame, at

FOUO 2025 06 24 15 00

about $t_1 + nH + 24.75\mu s$, and the signal HDCLK2 is used to update the crosspoints during the blanking interval of field 2 and has an active clock edge occurring halfway through line 563 of each frame, at about $t_1 + nH + 16,716.17\mu s$. The

5 switch point of field 1 therefore occurs halfway through line 1 and the switch point of field 2 occurs halfway through the first complete line of field 2.

It will therefore be seen that the two routers are operated without explicit regard to time relative to the

10 lines of the respective video signals but by establishing a time reference point and measuring lapse of time after the reference point.

The foregoing description of FIG. 1 has been based for convenience on the assumption that all the crosspoints of

15 each router are updated simultaneously. However, routers are available in which the crosspoints on a given input bus can be updated at a different time from the crosspoints on a different input bus. Such a router can be used for both the HD signals and the SD signals. FIG. 2 shows such an

20 arrangement. The SDCLK signals are used for updating the crosspoints on the router input buses that receive the SD signals and correspondingly the HDCLK signals are used for updating the crosspoints on the router input buses that receive the HD signals.

25 FIG. 3 illustrates schematically a post production facility having three video sources 34, more specifically designated Source P, Source Q and Source R which supply video signals in, respectively, NTSC, SMPTE format K and SMPTE format M. The three video signals are supplied to format

30 converters 38, 40 and 42 respectively. The converter 38 converts the NTSC signal to SMPTE format E and converts format E to SMPTE 292. The converter 40 converts SMPTE format K to SMPTE 292 and the converter 42 converts SMPTE format M to SMPTE 292.

35 The three sources 34 operate under control of a master clock generator 50, which generates a master clock MCLK at 60 Hz. The master clock signal is used directly to control Source P and Source R. A clock signal at 24 Hz is generated

1054279-0330-0624660

from the master clock signal by integer multiplication and division and is used to control Source Q. Since the same clock signal is used to control all three sources, it is straightforward to align line 1, field 1, frame 1 of the three sources at a reference time t_0 .

The master clock signal is also used to control the format converters, so that the output signals of the format converters are aligned at time t_1 , where $t_1 - t_0$ represents delay from the outputs of the sources 34 to the outputs of the format converters.

The three SMPTE 292 signals P, Q and R are supplied to a router 46, which selects among the three signals P, Q and R to generate output signals U and V. The switch points for the router 46 are determined based on lapse of time from the reference time t_1 . The first active edge of the master clock signal MCLK coincides with the start of line 1, field 1, frame 1 of the three signals P, Q and R.

The switch points for the interlaced format of signal P (format E) are halfway through line 1 and halfway through the first complete line of field 2. The field 1 switch points of format E are at $t_1 + (2n - 2) * H + 14.81\mu s$, where H is the period of the master clock signal and n is the frame number, and the field 2 switch points of format E are at $t_1 + (2n - 1) * H + 29.64\mu s$. Over a five frame sequence, the frame 1 switch point of signal Q, which is based on the progressive scan format K, is at $t_1 + 18.52\mu s$, the frame 2 switch point is at $t_1 + 2H + 8351.85\mu s$, the frame 3 switch point is at $t_1 + 5H$, the frame 4 switch point is at $t_1 + 7H + 8351.85\mu s$, and the frame 5 switch point is at $t_1 + 10H$. The frame n switch point of signal R, which is based on the progressive scan format M, is $t_1 + (n - 1) * H + 11.11\mu s$.

It can be seen from the foregoing that the time offsets of the switch points of the several formats are offset from the active clock edges of the master clock signal MCLK in a predictable and repeating fashion. It will be appreciated that similar considerations apply to a 25 Hz frame rate.

It has been assumed in the foregoing discussion that the value of M is one, not 1.001. Since each of the signal

105280-2624560

formats mentioned in the foregoing discussion has a frame rate that is not an integer number of frames per second but an integer divided by M frames per second, the time offsets mentioned above would have to be multiplied by M.

5 Further, although for the sake of simplicity the invention has been described with reference to controlling the router so that the switch line is the first line of the vertical blanking interval of each field, the switch line could equally well be another line of the vertical blanking
10 interval. It is necessary only that the several formats be aligned so that at an arbitrary time t_{ref} the beginning of a given line of each format is aligned in time with the beginning of a line of each other format. When this is achieved, the switch points can be controlled by measuring
15 lapse of time from the time t_{ref} , without regard to line count.

It will be appreciated that the invention is not restricted to the particular embodiment that has been described, and that variations may be made therein without
20 departing from the scope of the invention as defined in the appended claims and equivalents thereof.

06042797.032901